JC603 U.S. PTO
10/015169
10/23/01

PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10015169	10/23/2001	~~257~~ 345	~~64~~ 98	~~2816~~ 2675	~~STARK~~ Anyaso Lambert

**APPLICANTS: Kawahata Ken; Yamada Yukimitsu;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:
JAPAN 2000-324496 10/24/2000
JAPAN 2001-208160 07/09/2001

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☐ yes ☐ no	ATTORNEY DOCKET NO	
35 USC 119 conditions met	☐ yes ☐ no	9281-4195	
Verified and Acknowledged Examiners's intials			

TITLE : Shift register circuit including first shift register having plurality of stages connected in cascade and second shift register having more stages

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
	Assistant Examiner	Total Claims	Print Claim for O.G
ISSUE FEE		DRAWING	
Amount Due / Date Paid		Sheets Drwg. / Figs.Drwg. / Print Fig.	
☐ TERMINAL DISCLAIMER	Primary Examiner	Application Examiner	
	PREPARED FOR ISSUE		

WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.

FILED WITH: ☐ DISK (CRF) ☐ CD-ROM
(Attached in pocket on right inside flap)